REMARKS

This response is intended as a full and complete response to the final Office Action mailed August 24, 2004. In the Office Action, the Examiner noted that claims 27-35 and 48-54 are pending in the application, and that claims 27-35 and 48-54 are rejected under 35 U.S.C. §103. The Examiner also noted that the drawings are objected to because the first figure is not numbered. A replacement drawing which has been numbered is enclosed.

By this response, the Applicants have amended claims 27 and 48. In view of the above amendments and the following discussion, the Applicants submit that the claims pending in the application are believed to be non-obvious under 35 U.S.C. §103. Thus, the Applicants believe that the application is in condition for allowance.

IN THE DRAWINGS

The Examiner has objected to the drawings. Specifically, the Examiner states "[T]he drawings are objected to because the first (1st) figure is not numbered." A replacement first sheet of drawing amended to reflect that the figure is FIG. 1 is enclosed. The Applicants respectfully request that the Examiner's objection be withdrawn.

REJECTION OF CLAIMS UNDER 35 U.S.C. §103(a)

A. Claims 27-29, 31-35, 48-50, 53 and 54

The Examiner has rejected claims 27-29, 31-35, 48-50, 53 and 54 under 35 U.S.C. §103(a) as being unpatentable over Herrmann et al. (U.S. Patent No. 6,134,707, hereinafter "Herrmann") and further in view of Tang (U.S. Patent No. 6,389,321, hereinafter "Tang") and further in view of Sasaki (U.S. Patent 6,198,304, hereinafter "Sasaki"). The rejection is respectfully traversed.

The Applicants' independent claim 27 recites:

> "A method for programming one or more programmable logic devices, comprising:
> programming a first file in a non-native format for programming said one or more programmable logic devices from a remote programmer source;
> converting said non-native format programmable logic instructions into a second file having programmable logic instructions in a format native to said programmable logic device;
> transferring said second file to a server comprising a processor board coupled to a plurality of functional elements, each said functional element comprising a programmable logic device coupled to a switching circuit;
> executing said converted file, for identifying particular target files associated with said programmable logic devices, via a first bus coupled to said switching circuits;
> enabling switching circuits corresponding to said identified target files via said first bus; and
> programming said identified programmable logic devices via a second bus coupled to said switching circuit." (emphasis added).

The test under 35 U.S.C. §103 is not whether an improvement or a use set forth in a patent would have been obvious or non-obvious; rather the test is whether the claimed invention, considered as a whole, would have been obvious. Jones v. Hardy, 110 USPQ 1021, 1024 (Fed. Cir. 1984) (emphasis added). Thus, it is impermissible to focus either on the "gist" or "core" of the invention, Bausch & Lomb, Inc. v. Barnes-Hind/Hydrocurve, Inc., 230 USPQ 416, 420 (Fed. Cir. 1986) (emphasis added). Moreover, the invention as a whole is not restricted to the specific subject matter claimed, but also embraces its properties and the problem it solves. In re Wright, 6

USPQ 2d 1959, 1961 (Fed. Cir. 1988) (emphasis added). The combination of Herrmann, Tang and Sasaki fails to teach or suggest the Applicants' invention as a whole.

In particular, the Herrmann reference discloses a PCB 30 also includes an embedded controller 52 running interpreter software 54. The embedded controller preferably includes JTAG interface circuitry (not shown). A bus 56 is used to route programming signals from the embedded controller 52 to the IC 50 (see Herrmann, col. 4, lines 56-60 and FIG. 1).

Further, the Tang reference merely discloses that "the microprocessor, which executes a program stored in the non-volatile memory (e.g., EPROM 608), specifies an address on an address bus (e.g., address bus 604), so as to store data on the data bus to memory (e.g., RAM 607). The programming data stored in RAM 607 can be provided to ISP controller 402 via data bus 603 under the control of microprocessor 605, which provides a control signal 610 ("read/write") for latching the data into ISP controller 402." (See Tang, col. 5, lines 61-65 and col. 4, lines 49-53).

The Sasaki reference discloses "the Address Frame is a thirty-two-bit sequence that performs two functions. Primarily, the Address Frame contains address of the PLD 300, 400, 500a-c and 600a-c area to be programmed and that a data frame will be coming. This orders the programming circuit to switch from examining the thirty-two bit data streams to examining data streams as eight bit sequences" (see Sasaki, Column 13, Lines 52-58).

However, the combination of Herrmann, Tang and Sasaki fails to teach or suggest "transferring said second file to a server comprising a processor board coupled to a plurality of functional elements, each said functional element comprising a programmable logic device coupled to a switching circuit," or "executing said converted file, for identifying particular target files associated with said programmable logic devices, via a first bus coupled to said switching circuits," or "programming said identified programmable logic devices via a second bus coupled to said switching circuit."

That is, the Applicants' invention provides:

The processor 332 is electrically coupled to each circuit board 334 via board select bus 340 and a JTAG bus 342. In one embodiment, the board select bus 340 is a parallel bus, while the JTAG bus 342 is a serial bus.

Each circuit board 334 comprises circuitry including a PLD 338 and a corresponding switching circuit 336. The PLD 338 interacts with other circuitry (not shown) on the circuit card 334 to perform some function, task, or plurality of tasks. The board select bus 340 and JTAG bus 342 are coupled to inputs of the switching circuit 336 and provide input signals to the switching circuit 336." (see Applicants' specification, page 10 lines 9-23 and FIG. 3).

Furthermore, the Applicants' specification further provides that:

In step 412, the server receives the JBC file and the method 400 proceeds to step 414. In step 414, the processor (e.g., a plurality of processors arranged in a parallel) executes the JBC file to run the JBC program. In step 416, the JBC program identifies target files on each of the circuit boards having the programmable logic device (PLD). In particular, the JBC program is transferred over the board select bus, which is a parallel bus between the processor, and each circuit board coupled to the backplane. The executed program initially identifies those programming logic devices on the circuit boards that correspond to the JBC program (e.g., a particular programmable logic device type or family of devices of a specific manufacturer).

In step 418 the JBC program marks the identified target files (PLDs) by enabling the switching circuit on the circuit board. Specifically, the JBC program marks the PLD target files that require an upgrade (i.e., reprogramming). Once the switching circuit corresponding to the identified target files are set in an enabling mode, then, in step 420, the JBC program is transferred to the corresponding PLD's requiring an update via the JTAG bus. Specifically, in step 422, the switching circuits that have been enabled, transfer the JBC program from the processor board 332, via the JTAG bus, to the PLD. In step 424, the particular PLD's marked for an update receive the JBC program, whereupon the program is executed to modify the operational parameters according to the programming initially created by the programmer in the programmer object file (POF). (see Applicants' specification, page 11, line 30 to page 12, line 26, and FIGS. 4A and 4B).

Even if the three references could somehow be operably combined, the combination merely discloses a controller coupled to a programmable logic device via a control path and a data path, and a switching circuit to switch from examining a 32-bit sequence to examining an 8-bit sequence. That is, the combined references merely disclose when the PLD detects a predefined pattern of a start frame, programming of the PLD commences. The switching circuitry merely enables 8-bit data to be examined,

instead of 32-bit data. By contrast, the Applicants' invention includes "enabling switching circuits corresponding to said identified target files via said first bus," and "programming said identified programmable logic devices via a second bus coupled to said switching circuit". In other words, these switching circuits are enabled via a first bus, and once enabled, the identified programmable logic devices are programmed via a second bus, which is also coupled to the switching circuit. Therefore, the combined references fail to teach or suggest the Applicants' invention as a whole.

In light of the reasons given above, it is respectfully submitted that Herrmann, Tang or Sasaki, singly or in combination, fail to teach, show or suggest Applicants' invention as defined by independent claim 27. Accordingly, independent claim 27 is believed to be nonobvious and allowable under 35 U.S.C. §103.

Furthermore, claims 28-29 and 31-35 depend directly or indirectly from independent claim 27 and recite additional features thereof. As such, and at least for the same reasons set forth above with respect to Applicants' independent claim 27, the Applicants submit that these claims are also non-obvious and allowable under 35 U.S.C. §103. Therefore, the Applicants respectfully request that the rejections be withdrawn.

2. Claims 48-50, 53 and 54

Applicants' independent claim 48 recites:

> "An apparatus for programming at least one programmable logic devices, comprising:
>
> at least one circuit board respectively comprising said at least one programmable logic device respectively coupled to at least one switching circuit;
>
> a processor system coupled to said at least one switching circuit via a board select bus and a JTAG bus, said processor system for receiving from a remote source, a file in a format native to said at least one programmable logic device; and
>
> wherein said processor system executes said file in a format native to said at least one programmable logic device, and selectively enables said at least one switching circuit via the board select bus for programming an associated programmable logic device via said JTAG bus." (emphasis added).

As discussed above, the Herrmann reference discloses a PCB 30 also includes an embedded controller 52 running interpreter software 54. The embedded controller preferably includes JTAG interface circuitry (not shown). A bus 56 is used to route programming signals from the embedded controller 52 to the IC 50 (see Herrmann, col. 4, lines 56-60 and FIG. 1).

Further, the Tang reference merely discloses that "the microprocessor, which executes a program stored in the non-volatile memory (e.g., EPROM 608), specifies an address on an address bus (e.g., address bus 604), so as to store data on the data bus to memory (e.g., RAM 607). The programming data stored in RAM 607 can be provided to ISP controller 402 via data bus 603 under the control of microprocessor 605, which provides a control signal 610 ("read/write") for latching the data into ISP controller 402." (See Tang, col. 5, lines 61-65 and col. 4, lines 49-53).

Thus, the combined references merely disclose a controller coupled to a programmable logic device via a control path and a data path. However, the combined references fail to teach or suggest "said processor system executes a file in a format native to said at least one programmable logic device, selectively enables said at least one switching circuit via the board select bus for programming an associated programmable logic device via said JTAG bus."

That is, the Herrmann and Tang references fail to teach or suggest that a switching circuit is turned on and off via a first signal path, and the programmable logic device is programmed by sending program information via a second bus (i.e., JTAG bus) and the switching circuit, which transfers the information to the programmable logic device (PLD).

Furthermore, the Sasaki reference fails to bridge the substantial gap as between the Hermann and Tang references and the Applicants' invention. In particular, the Sasaki reference discloses "the Address Frame is a thirty-two-bit sequence that performs two functions. Primarily, the Address Frame contains address of the PLD 300, 400, 500a-c and 600a-c area to be programmed and that a data frame will be coming. This orders the programming circuit to switch from examining the thirty-two bit data

streams to examining data streams as eight bit sequences." (See Sasaki, col. 13, lines 52-58).

Even if the three references could somehow be operably combined, the combination would disclose a controller coupled to a programmable logic device via a control path and a data path, and a switching circuit for switching to an 8-bit data stream from a 32-bit data stream. This is completely different from the Applicants' invention. The Applicants' invention uses a switching circuit to enable data to be sent on a second bus to the PLD. That is, the switching circuit of the Applicants' invention turns on and off the JTAG bus. By contrast, the combined references teach away from the Applicants' invention, since the PLD (of Sasaki) will always receive a data signal over the signal path via the switching circuit. That is, the switching circuit taught by Sasaki only provides a routing function, as opposed to enabling/disabling the signal path. Therefore, the combined references fail to teach or suggest the Applicants' invention as a whole.

As such, Applicants submit that independent claim 48 is not obvious and is fully patentable under 35 U.S.C. §103 over the combined references. Furthermore, Claims 49-50, 53 and 54 depend, either directly or indirectly, from independent claim 48 and recite additional features thereof. As such, and for at least the same reasons as discussed above with respect to independent claim 48, the Applicants submit that these dependent claims are also not obvious and patentable under 35 U.S.C. §103 over the combined references. Therefore, the Applicants respectfully request that the rejections be withdrawn.

B. Claim 52

The Examiner has rejected claim 52 under 35 U.S.C. §103(a) as being unpatentable over Herrmann, Tang, Sasaki and further in view of admitted prior art. Applicants respectfully traverse the rejection.

Claim 52 is dependent directly upon independent claim 48. For at least the same reasons discussed above with respect to independent claim 48, dependent claim 52 is patentable under 35 U.S.C. §103(a) over Herrmann, Tang and Sasaki alone or in combination.

The Examiner contends that "... admitted prior art discloses in an analogous computer system wherein said at least one programmable logic device is selected from the group consisting a gate array, field programmable gate array, programmable, field programmable logic array, read only memory, programmed array logic, programmable logic array, and complex programmable logic devices...." and that "[T]herefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the selecting of devices is selected from the group comprising gate array as taught in admitted prior art in corresponding to programming PLD as taught in combination system by Herrmann, Tang, and Sasaki...."Applicants respectfully disagree.

In particular, the combination of Hermann, Tang, Sasaki and the Applicants' admitted prior art (AAPA) merely discloses a controller coupled to a programmable logic device via a control path at a data path, and a switching circuit for switching to an 8-bit data stream from a 32-bit data stream. Nowhere in the combined references is there any teaching or suggestion of "said processes system executes said file in a format native to said at least one programmable logic device, and selectively enables said at least one switching circuit via the board select bus for programming and associated programmable logic device via said JTAG bus." Therefore, the combined references fail to teach or suggest the Applicants' invention as a whole.

As such, Applicants submit that dependent claim 52 is not obvious and patentable under 35 U.S.C. §103 over the combination of Herrmann, Tang, Sasaki and further in view of admitted prior art. Therefore, the Applicants respectfully request that the rejection be withdrawn.

C. Claims 30 and 51

The Examiner has rejected claims 30 and 51 under 35 U.S.C. §103(a) as being unpatentable over Herrmann, Tang, Sasaki in view of technical paper published in May 1999, ver. 6, hereinafter called Altera Corporation. Applicants respectfully traverse the rejection.

Claims 30 and 51 respectively depend directly from independent claims 27 and 48 and recite additional features thereof. As discussed above, the combination of Herrmann, Tang and Sasaki alone and in combination fail to teach or suggest the Applicants' invention as a whole. Specifically, the three references fail to teach or suggest the claimed features of "enabling switching circuits associated with identified programmable logic devices associated with said particular target files via said first bus," and "wherein said processor system executes said file in a format native to said at least one programmable logic device, and selectively enables said at least one switching circuit via the board select bus for programming an associated programmable logic device via said JTAG bus".

Furthermore, the Altera reference fails to bridge the gap as between the three references and the Applicants' invention. In particular, the Altera reference merely discloses that "[t]he Jam standard is a vendor- and platform-independent interpreted language optimized for programming devices via the IEEE std. 1149.1 (JTAG) interface. The Jam language allows a single Jam file (.jam) or Jam Byte-Code file (.jbc) to contain both the data to be programmed into a device and the algorithm required to accomplish programming." (see Altera, page 7, first paragraph).

However, the Altera reference in combination with the Herrmann, Tang and Sasaki references is completely silent with respect to the claimed features of "enabling switching circuits associated with identified programmable logic devices associated with said particular target files via said first bus," and "wherein said processor system executes said file in a format native to said at least one programmable logic device, selectively enables said at least one switching circuit via the board select bus for programming an associated programmable logic device via said JTAG bus". Therefore, the combined references fail to teach or suggest the Applicants' invention as a whole.

Therefore, Applicants submit that claims 30 and 51 are not obvious and are patentable under 35 U.S.C. §103 over the combined references. Therefore, the Applicants respectfully request that the rejections be withdrawn.

THE SECONDARY REFERENCES

The secondary references made of record are noted. However, it is believed that the secondary references are no more pertinent to the Applicant's disclosure than the primary references cited in the Office Action. Therefore, Applicants believe that a detailed discussion of the secondary references is not necessary for a full and complete response to this Office Action.

CONCLUSION

In view of the foregoing amendments and remarks, Applicants respectfully submit that the claims presently in this application are not obvious under the provisions of 35 U.S.C. §103. Applicants believe that this application is in condition for allowance. Reconsideration of this application and its swift passage to issue are respectfully solicited.

If, however, the Examiner believes that there are any unresolved issues requiring adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Eamon J. Wall or Steven M. Hertzberg at (732) 530-9404

so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,

10/25/04

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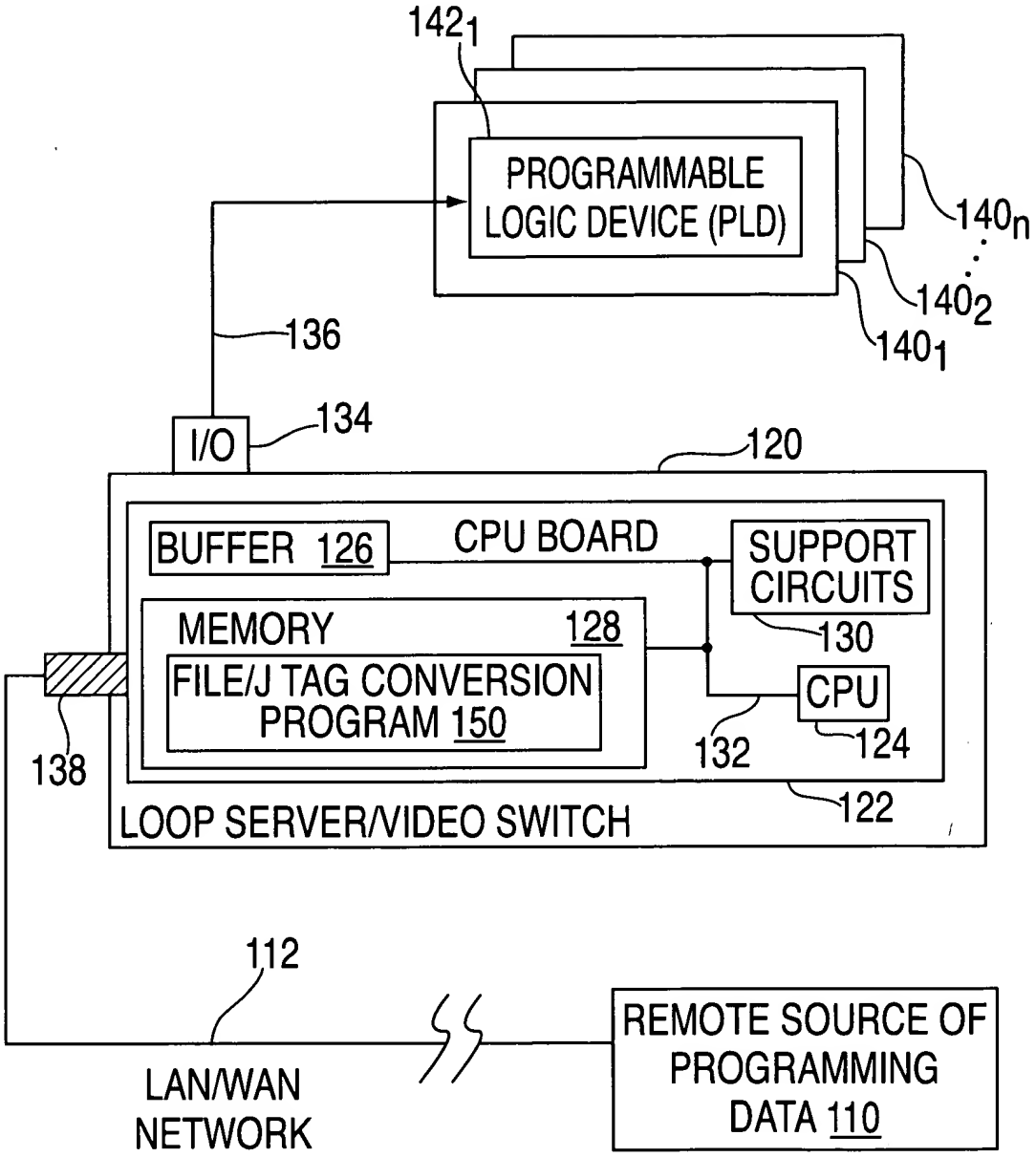

FIG. 1

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